**[On Chip Sensors for Process, Aging and Environmental Variations](https://venividiwiki.ee.virginia.edu/twiki/bin/view/Main/ClassECE6332Fall10GroupVariationandAgingMonitor" \o "On Chip Sensors For Process, Aging and Environmental Variations)**

**Design Project Proposal**

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Process and environmental variations are unavoidable realities that must be considered when designing any integrated circuit. As device scaling continues, it is becoming increasingly difficult to control circuit parameters such as doping levels, dopant distribution, and oxide thickness consistently. This results in varying levels of uncertainty in the global (die-to-die) and local (within-die) circuit performance. Characterizing these variations is an important practice that is essentially required to maintain reliable circuit performance and functionality as devices continually shrink and variations become more significant. These variations primarily manifest themselves as shifts in the transistor threshold voltage values [4]. Temporal threshold voltage variations can also result from changes in chip temperature and long-term device degradation processes such as Negative Bias Temperature Instability (NBTI) [5].

Many circuits that monitor process variation employ simple ring oscillators and frequency detectors. The variation of the ring oscillator frequency is a measure of the global variations of the devices on the die. To measure local device variations people in the past have placed large transistor arrays on a die and individually measured the characteristics of each device. Reference [3] is an example of such a circuit. This method can require hours of costly testing after the device has been fabricated. In [1], a ring oscillator circuit has been altered to give the oscillation frequency the ability to be used as a measure of local NMOS variation, local PMOS variation, or global device variation. This circuit will drastically reduce the area overhead and required test time compared to the large array circuits.

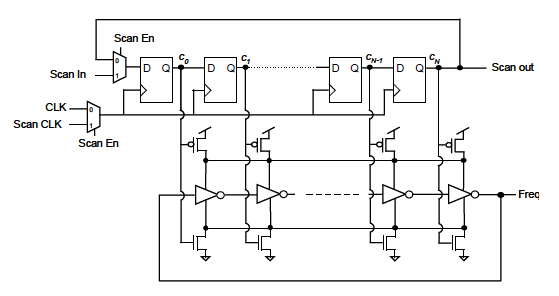


Figure 1 - Local Variation Detector from [1]

Because of the static nature of process variations, the oscillator circuit in [1] will also have the ability to be used as a sensor for temperature variation and NBTI degradation. After the initial local process variations are determined, the deviation from the expected values of the ring oscillator frequency can be used to characterize temperature gradients across the chip (Figure 2). NBTI degradation, which causes device characteristics to change over the course of years, can be measured in the same manner. In order to be able to separate the effects of NBTI degradation from the temperature effects, two ring oscillators must be used. Only one will place the PMOS devices under negative bias conditions. When measuring NBTI degradation, both oscillators will be turned on, and the difference between the two frequencies will negate out the process variations. Hence the amount of degradation resulting in the frequency mismatch will be only due to NBTI effect. This idea of beat frequency degradation has been described in [2]. Our project is to design and test one circuit (based on the basic idea from Figure 1) that can accurately and precisely measure local and global process variation and also sense temperature gradients and device degradation.

C:\Users\jar3qf\Documents\Variation Project\Pictures\temp variation vs freq edited.tif

Figure 2 - Ring Oscillator Frequency for Various Temperatures

Our simulation of the circuit in Figure 1 show that the device works as it should. Varying the number of devices that are on between the ring oscillator and the virtual rails changes the voltage level at the rails, which in turn affects the frequency. These results are collected in Table 1.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **1 PMOS On** | **6 PMOS On** | **1 NMOS On** |
| **Period** | 130.76 ps | 122.71 ps | 144.39 ps |
| **Frequency** | 7.6476 GHz | 8.149 GHz | 6.926 GHz |
| **Virtual VDD** | 0.965 V | 1.07 V | 1.1 V |
| **Virtual Gnd** | 0V | 0.03 V | 0.2495 V |

Table 1 - Preliminary Simulation Results for Circuit in Figure 1

The frequency detector connected to the ring oscillator determines the resolution of the output. This device needs to be carefully designed to ensure that it is able to detect even minute changes in the output frequency. Our project will include several different designs and tests to determine which one delivers the highest resolution while minimizing the area overhead. When measuring the frequency changes of just one of the oscillators, we could design a device to count positive edges that is enabled for the duration of a given input pulse. By keeping the enable duration constant, we can measure the difference in frequency as a difference of the counter values. We can double the resolution by incrementing the counter on both positive and negative edges. The resolution will also increase as the enable pulse duration increases. Because measuring the NBTI degradation requires the difference of two frequency outputs, two counters will be needed. The authors in [2] designed a high resolution circuit that acquires its output from the beat frequency of the two oscillators. All of these options will be explored.

We will also need to perform some sensitivity analysis to ensure that the frequency is primarily dependent on variations in the devices providing virtual Vdd and virtual Gnd to the ring oscillator. We will alter the sizes of the different devices in the structure and watch how the frequency of the oscillator changes with variations in the virtual rail transistors. We will attempt to extract the ideal sizing combination to maximize the efficacy of our design.

We will perform our simulations with several different CMOS technologies. This will allow us to show how the circuit’s performance changes with scaling to help predict the circuit’s performance in future technologies.

**Timeline**

*Week of Oct. 17th* – Do sensitivity analysis to determine ideal device sizing; design and test various frequency detectors

*Week of Oct. 24th* – Finalize frequency detector design; decide on ideal number of stages in ring oscillator for statistical significance

*Week of Oct. 31st* – Compile results into Design Review 2; run Monte Carlo simulations

*Week of Nov. 7th* – Organize Monte Carlo results into useful data

*Week of Nov. 14th* - Run simulations on finalized design with various technologies

*Week of Nov. 21st* – Develop final report and presentation

*Week of Nov. 28th* – Finalize report and practice presentation

**Task Breakdown**

Although all parts of the project will be worked on by both students, each will have a different area of focus. Jared will work on the NBTI aspect of the project, including the design of the differential frequency detector. Kaushik will focus on the process variation, ensuring that the Monte Carlo simulations are set-up and run correctly. He will also compile and organize the results.

**References**

1. **Agarwal, Kanak, “On-die sensors for measuring process and environmental variation in integrated circuits.” IBM Corps. Austin, TX. 2010.**
2. **Tae-Hyoung Kim; Persaud, R.; Kim, C.H.; "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," *Solid-State Circuits, IEEE Journal of* , vol. 43, no. 4, pp. 874-880, April 2008.**
3. **Kanak Agarwal , Sani Nassif, “Characterizing process variation in nanometer CMOS”, Proceedings of the 44th annual conference on Design automation, June 04-08, 2007, San Diego, California.**
4. **Natarajan, S.; Breuer, M.A.; Gupta, S.K.; , "Process variations and their impact on circuit operation," *Defect and Fault Tolerance in VLSI Systems, 1998. Proceedings., 1998 IEEE International Symposium on* , vol., no., pp.73-81, 2-4 Nov 1998.**
5. **M. A. Alam, S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," Microelectronics Reliability, vol. 45, pp. 71--81, 2005.**